Appl. No.

09/754,406

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AMENDMENTS TO THE DRAWINGS

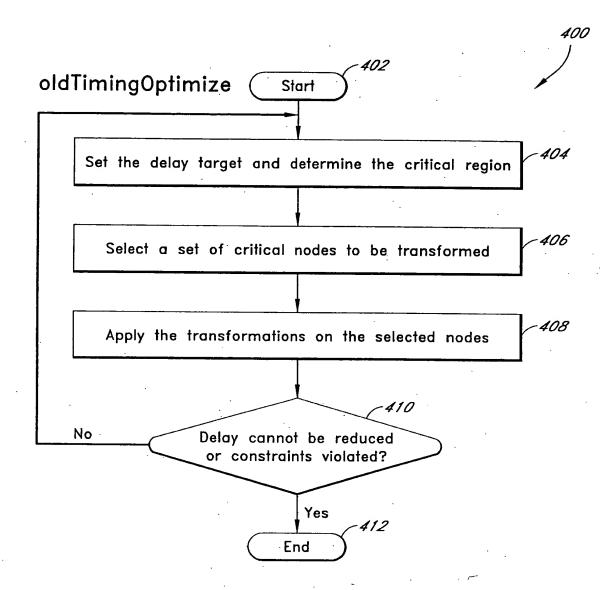
Applicant has amended Figure 2 as shown in the Replacement Sheet for Figure 2. Specifically, the legend –Prior Art—is added as requested by the Examiner.

METHODOLOGY AND APPLICATIONS OF TIMING-DRIVEN LOGIC RESYNTHESIS FOR VLSI CIRCUITS

Songjie Xu

Appl. No.: 09/754,406 · Atty Docket: APLUS.001A
Replacement Sheet





PRIOR ART

FIG. 2